GAUSSIAN FREQUENCY SHIFT KEYING DIGITAL DEMODULATOR

REFERENCE TO RELATED APPLICATIONS

[001]   This application is based on U.S. Provisional application Serial No. 60/466,684, filed April 29, 2003, entitled "GFSK Digital Demodulator for Bluetooth", incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

[002]   The present invention relates to the field of data communications and more particularly relates to a digital demodulator for use in a digital Gaussian frequency shift keying (GFSK) receiver such as a receiver constructed according to the Bluetooth standard.

BACKGROUND OF THE INVENTION

[001] In digital communications systems, a carrier signal is modulated with the digital data to be transmitted over the channel, where it typically suffers various forms of distortion, such as additive noise. The digital data is often transmitted in bursts wherein each burst consists of a number of data bits. Upon reception, the signal must be demodulated in order to recover the transmitted data.

[003]   It is common for receivers to employ direct conversion (i.e. homodyne receiver) to perform the demodulation of the received signal. The received signal is mixed with a local oscillator signal at the carrier frequency to produce I (in-phase) and Q (quadrature) baseband signals. An advantage of direct conversion receivers is that they are efficient in terms of cost and current consumption. The advantage is derived from having the incoming RF signal directly downconverted to baseband, in both I and Q components, without use of any IF frequencies.

[004]   In other receivers, the incoming RF signal is mixed down first to an intermediate frequency (IF) signal and subsequently to baseband. The IF frequency may be any convenient frequency. For example, in a Bluetooth receiver, the front-end may output a low frequency IF signal (e.g., Near-Zero IF) as low as half the bandwidth of the signal (i.e. 0.5 MHz in this case).

[005]   Considering Gaussian FSK (GFSK) modulation and considering the presence of frequency offsets, the zero-IF I and Q signals can be expressed mathematically by the following.

$$I_{ZIF} = A\cos\left[\varphi(t) + \Delta\omega_{IF}t + \theta_n\right]$$
$$Q_{ZIF} = A\sin\left[\varphi(t) + \Delta\omega_{IF}t + \theta_n\right]$$

$$(1)$$

where A is a constant, $\Delta\omega_{IF}$ represents the frequency offset, $\varphi(t)$ represents the phase shift created by the modulating data and θ_n represents the contribution of random noise to the phase. Note that it is

assumed there is no gain or phase mismatch. In Bluetooth low-IF systems, ω_{IF} is usually 500 kHz and the local oscillator frequency used for downconversion from RF to IF is given by $LO = \omega_C - \omega_{IF}$ where ω_c denotes the carrier frequency. The downconverted I signal is expressed mathematically as follows.

$$I = A\cos(\omega_{IF}t + \varphi(t) + \theta) \tag{2}$$

After downconversion from IF to zero-IF, the output signal is given by

$$I = A\cos(\varphi(t) + \theta) \tag{3}$$

Differential detection of this signal calculates

$$(\varphi(t) + \theta(t)) - (\varphi(t - T) + \theta(t - T)) \Rightarrow \Delta\varphi \tag{4}$$

where T represents the symbol time. In Bluetooth systems, the symbol time T is 1 microsecond. The result of differential detection yields $\sin(\Delta\varphi)$, which for small values of φ can be approximated as simply $\Delta\varphi$.

[006]   Numerous prior art analog techniques are available to perform the demodulation required to generate accurate output data. The modern trend, however, is to provide single chip solutions to communication applications. This requires all digital realization of all or most of the receiver circuitry in the radio. Digital realization of the radio for inclusion in single chip implementations is desirable because it offers a high performance solution at low current consumption and low gate count and hence reduced size and cost. These benefits are driving the current trend to realize as much of the radio digitally for placement on a single chip.

[007]   Any digital demodulator implementation, in particular digital demodulation of GFSK, must be able to perform in the presence of additive white Gaussian noise (AWGN), interference and frequency offsets. Frequency offsets are another form of distortion of the received signal, since they are random and must be resolved adequately in the receiver to minimize the performance degradation they cause. Considering a communication system constructed to receive GFSK in accordance with the Bluetooth standard, the receiver must be constructed to deal with frequency offsets in order to generate a reliable output signal. There exist several sources of frequency offset errors in a Bluetooth communication system as highlighted below.

[008]   First, the Bluetooth specification permits a frequency error of up to 75 kHz in the transmitted signal. Second, the Bluetooth specification also permits up to 20 ppm of frequency inaccuracy in the receiver crystal reference, which could result in up to 50 kHz of frequency offset in the receiver's local oscillator which is used in the downconversion. Further, an additional frequency offset of up to 40 kHz is allowed in the transmitted signal during transmission of long packets. Lastly, an

additional 15 kHz of frequency offset may be due to clock jitter caused by using clocks derived from dividing the master local clock signal, wherein the local clock signal is hopping from frequency to frequency resulting in jitter. This frequency offset could be avoided by using more accurate clocks without clock division. Note that the first two frequency offsets are constant in nature and due to the open loop configuration of the transmitter permitted under the Bluetooth standard.

[009]   Thus, an IF signal at the receiver's demodulator input may have a total of up to 180 kHz in frequency offset. Considering a nominal frequency deviation of +/-160 kHz for a modulation index of h=0.32, in accordance with the Bluetooth specification, a possible frequency offset of 180 kHz makes reception virtually impossible. Note that using a lower modulation index of 0.28, which the Bluetooth specification allows, makes the problem even worse.

[0010]   Thus, there is a need for a digital demodulator, suitable for single chip implementations, that meets the requirements of the Bluetooth specification and that overcomes the problems and disadvantages of the prior art.

SUMMARY OF THE INVENTION

[0011]   The present invention solves the problems of the prior art by providing a digital demodulator employing a digital differential detection mechanism. The mechanism is based on extracting phase differences directly from the I and Q signals after downconversion to zero-IF and image rejection are performed. The phase φ represented by the quadrature I and Q signals is determined using the relationship $\varphi = \arctan\left(\dfrac{Q}{I}\right)$. A lookup table stores the values of the arctan function preferably in a reduced size format. The size of the lookup table can be reduced significantly by storing arctan values for the first quadrant only (i.e. 0 to 90°) and taking advantage of the fact that the phase values for the other three quadrants can be derived from those of the first by separately considering the magnitude and the sign of the I and Q samples. Phase extraction logic is provided that is operative to map the phase into the entire 0 to 360° range of phase values (i.e. $-\pi$ to $+\pi$ radians) based on the signs of the I and Q signals.

[0012]   In addition to the reduction of the lookup table size by a factor of four (i.e. only a quarter of the range needs to be covered due to the use of the phase extraction logic), further optimization of the lookup table is made regarding the quantization/resolution of its contents. In particular, the required size of the lookup table in an example embodiment presented herein is only 225 words (i.e. bytes). The reduction in the size of the lookup table is achieved by the use of a per sample scaler that functions to compress a 16-bit input into a 5-bit output while maintaining the $\dfrac{Q}{I}$ ratio at a sufficient accuracy that does not compromise receiver performance.

[0013]   An additional digital processing block is used to determine the phase differences between a current phase value and the previous phase value. It is these phase differences that reflect the frequency deviations present in the received signal which represent the original modulating signal. Further, a 'clicks' filter circuit is provided that is operative to remove the discontinuities in the phase difference output that occur around 2π radians.

[0014]   Several advantages of the digital demodulator of the present invention include the ability to be implemented in a very small size, and therefore low cost, compared with prior art solutions. In addition, the mechanism is operative to extract actual phase differences wherein frequency offsets are translated to DC offsets, thereby greatly simplifying frequency offset compensation in subsequent processing. This is in comparison to prior art differential demodulators which typically generate the sine, cosine or other nonlinear function of the phase difference, which greatly

complicates frequency offset estimation and compensation resulting in either added complexity or degraded performance for certain values of frequency offsets.

[0015] Another advantage of the mechanism of the present invention is that phase extraction is operative to generate signals with linear noise terms. This is in contrast to prior art solutions wherein the resultant noise terms are nonlinear and correlated to the data due the multiplications typically performed. Linearity of the noise in the presence of intersymbol interference (ISI) serves to simplify the realization of equalizers placed after the demodulator and provide enhanced performance.

[0016] A further advantage of the mechanism is that the it enables subsequent frequency offset compensation that can be implemented very simply and which can be performed in a feed forward manner without requiring a closed loop architecture. Since frequency offsets are translated into DC offsets, the frequency offsets are easier to extract and suppress as compared to prior art cross-multiply architectures typically used for digital demodulation, which have the disadvantage of introducing distortion when frequency offsets are present.

[0017] Note that many aspects of the invention described herein may be constructed as software objects that are executed in embedded devices as firmware, software objects that are executed as part of a software application on either an embedded or non-embedded computer system running a real-time operating system such as WinCE, Symbian, OSE, Embedded LINUX, etc. or non-real time operating system such as Windows, UNIX, LINUX, etc., or as soft core realized HDL circuits embodied in an Application Specific Integrated Circuit (ASIC) or Field Programmable Gate Array (FPGA), or as functionally equivalent discrete hardware components.

[0018] There is therefore provided in accordance with the invention, a differential detector for use in a digital frequency shift keying (FSK) receiver comprising first means for receiving a scaled I signal and a scaled Q signal and determining the absolute value thereof to yield an absolute scaled I signal and an absolute scaled Q signal, an arctan lookup table (LUT) for outputting a first phase value in accordance with each absolute scaled I signal and absolute scaled Q signal pair and second means for generating a delta phase value in accordance with the first phase value and a previous first phase value delayed one symbol time.

[0019] There is also provided in accordance with the invention, a method of differential detection for use in a digital frequency shift keying (FSK) receiver, the method comprising the steps of receiving a scaled I signal and a scaled Q signal and determining the absolute value thereof to yield an absolute scaled I signal and an absolute scaled Q signal, providing an arctan lookup table (LUT) adapted to output a preliminary phase value in the range of 0 to $\frac{\pi}{2}$ in accordance with each absolute

scaled I signal and absolute scaled Q signal pair, determining a resolved phase value in the range of $-\pi$ to $+\pi$ in accordance with the sign of the scaled I signal and the scaled Q signal and generating a delta phase value in accordance with the resolved phase value and a previous resolved phase value delayed one symbol time.

[0020]   There is further provided in accordance with the invention, a differential demodulator for use in a digital frequency shift keying (FSK) receiver comprising first means for receiving a scaled I signal and a scaled Q signal and determining the absolute value thereof to yield an absolute scaled I signal and an absolute scaled Q signal, second means for providing an arctan lookup table (LUT) adapted to output a first phase value in the range of 0 to $\dfrac{\pi}{2}$ in accordance with each absolute scaled I signal and absolute scaled Q signal pair, third means for determining a second phase value in the range of $-\pi$ to $+\pi$ in accordance with the sign of the scaled I signal and the scaled Q signal and fourth means for generating a delta phase value in accordance with the second phase value and a previous second phase value delayed one symbol time.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021]   The invention is herein described, by way of example only, with reference to the accompanying drawings, wherein:

[0022]   Fig. 1 is a block diagram illustrating an example GFSK receiver including a digital demodulator constructed in accordance with the present invention;

[0023]   Fig. 2 is a block diagram illustrating the baseband scaler portion of the GFSK receiver in more detail;

[0024]   Fig. 3 is a pseudo code listing illustrating the selection logic portion of the baseband scaler in more detail;

[0025]   Fig. 4 is a block diagram illustrating the arctan differential detector portion of the GFSK receiver in more detail;

[0026]   Fig. 5 is a table illustrating the contents of the arctan look up table used in the arctan differential detector;

[0027]   Fig. 6 is a pseudo code listing illustrating the handling of the special cases where the row and/or column index is zero;

[0028]   Fig. 7 is a graph of the I/Q plane illustrating the range covered by the arctan look up table;

[0029]   Fig. 8 is a pseudo code listing illustrating the operation of the phase extractor portion of the Arctan differential detector; and

[0030]   Fig. 9 is a pseudo code listing illustrating the operation of the 'clicks' filter portion of the arctan differential detector.

DETAILED DESCRIPTION OF THE INVENTION

Notation Used Throughout

The following notation is used throughout this document.

Term	Definition
AFC	Automatic Frequency Control
AHDL	Adaptive Hard Decision Logic
ASIC	Application Specific Integrated Circuit
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
DC	Direct Current
FPGA	Field Programmable Gate Array
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
HDL	Hardware Description Language
IF	Intermediate Frequency
ISI	Intersymbol Interference
LO	Local Oscillator
LSB	Least Significant Bit
LUT	Look-Up Table
MSB	Most Significant Bit
RAM	Random Access Memory
ROM	Read Only Memory
RF	Radio Frequency

Detailed Description of the Invention

[0031] The mechanism of the present invention is based on extracting phase differences directly from the I and Q signals after downconversion to zero-IF and image rejection are performed. The phase φ represented by the quadrature I and Q signals is determined using the relationship $\varphi = \arctan\left(\frac{Q}{I}\right)$.

A lookup table stores the values of the arctan function preferably in a reduced size format. The size of the lookup table can be reduced significantly by storing arctan values for the first quadrant only (i.e. 0 to 90°) and taking advantage of the fact that the phase values for the other three quadrants can be derived from those of the first by separately considering the magnitude and the sign of the I and Q samples. Phase extraction logic is provided that is operative to map the phase into the entire 0 to 360° range of phase values (i.e. $-\pi$ to $+\pi$ radians) based on the signs of the I and Q signals.

[0032] In addition to the reduction of the lookup table size by a factor of four (i.e. only a quarter of the range needs to be covered due to the use of the phase extraction logic), further optimization of the

lookup table is made regarding the quantization/resolution of its contents. In particular, the required size of the lookup table in an example embodiment given is only 225 words (i.e. bytes). The reduction in the size of the lookup table is achieved by the use of a per sample scaler that functions to compress a 16-bit input into a 5-bit output while maintaining the $\frac{Q}{I}$ ratio at a sufficient accuracy which does not compromise receiver performance.

[0033]   An additional digital processing block is used to determine the phase differences between a current phase value and the previous phase value. It is these phase differences that reflect the frequency deviations present in the received signal which represent the original modulating signal. Further, a 'clicks' filter circuit is provided that is operative to remove the discontinuities in the phase difference output that occur around 2π radians.

[0034]   The mechanism can be used, as shown in an example embodiment, in a multi-stage scheme to perform differential detection of the I and Q input signals. The present invention is well suited for use in a digital FSK receiver such as a Gaussian Frequency Shift Keying (GFSK) detector constructed according to the Bluetooth specification.

[0035]   It is noted that the present invention is not limited to use with any particular modulation or communication system. Throughout this document the invention is described in reference to a Bluetooth communication system. Note that the invention is not limited to this communications system, as one skilled in the relevant electrical arts can apply the digital demodulator with arctan based differential detector mechanism of the present invention to other communication systems without departing from the spirit and scope of the present invention. Depending on the particular application and implementation, the invention is applicable for use in a multitude of communication systems, modulations and protocols. In general, the digital demodulator with arctan based differential detector mechanism of the present invention is applicable in systems where it is desirable to have frequency offsets translated to DC offsets, so as to simplify their suppression, such as in Bluetooth systems. Such needs may be encountered not only in wireless communication systems, such as those based on the Bluetooth standard, but also in non-wireless or non communication systems.

[0036]   A block diagram illustrating an example GFSK receiver including a digital demodulator constructed in accordance with the present invention is shown in Figure 1. The example receiver, generally referenced 10, comprises an Rx front end portion 11 and Rx demodulator portion 13. The Rx front end portion comprises an antenna 12, RF front end circuit 14 including analog to digital converter 16 for the inphase I signal and analog to digital converter 18 for the quadrature phase Q

signal. The outputs of the Rx front end are the IF I and Q signals, I_{IF} and Q_{IF}. The Rx demodulator comprises IF normalizer 20, IF to baseband converter 22, baseband scaler 24, differential detector 26, automatic frequency control (AFC) 28, adaptive hard decision logic (AHDL) 30 and filter 32. The data out signal is the recovered original signal, which was encoded, modulated and transmitted by the transmitter. Depending on the level of signal and interference received at the antenna, this recovered signal may have between 0 and 50% of erroneous bits in it when compared with the original data transmitted.

[0037]   The RF front end performs the amplification, mixing and filtering functions to generate both the I and Q signal paths. The I and Q signals are converted to digital form by analog to digital converters 16, 18. The resulting I_{IF} and Q_{IF} digital signals are input to the IF normalizer, which is responsible for several tasks including DC offset compensation, prescaling and Automatic Gain Control (AGC) management for the entire receiver. Note that the term normalizer is intended to indicate that the IF signals are processed in order to bring their amplitudes to within a predefined working region such that they may be handled properly by subsequent processing stages within the GFSK demodulator 13.

[0038]   The operation of the baseband scaler will now be described in more detail. A block diagram illustrating the baseband scaler portion of the GFSK receiver in more detail is shown in Figure 2. The adaptive baseband scaler module is operative to reduce the resolution of the I and Q signals from their nominal width of 16-bits signed to 5-bits signed while (1) maintaining the ratio of $\frac{Q}{I}$ which is required for the proper operation of the arctan differential detector 26 (Figure 1); and (2) preserving sufficient content to obtain sufficient phase resolution from the arctan differential detector. The reduction in resolution enables the size of the detector to be significantly reduced.

[0039]   The baseband scaler, generally referenced 24, comprises an absolute function 40, 42 for the baseband I and Q signals I_{BB} and Q_{BB}, respectively, multiplexer 44, comparator 46, selection logic 48, multiplexers 50, 56 and limiters 52, 54. The baseband scaler functions to determine the five highest active bits of I_{BB} and Q_{BB} during each sample and to output them as scaled baseband values I_{SBB} and Q_{SBB}. The selection of the five most active bits to route from the 16-bit full resolution I and Q signals is made according to the signal having the larger absolute value at each specific sample time. The logic in this block is preferably combinatorial since each I/Q sample pair generates a potentially different routing. The scaled baseband I and Q signals must be limited to ±15 (i.e. 4-bits in magnitude) for the subsequent detection stage.

[0040]   In operation, the baseband scaler first determines the absolute value of the baseband I and Q signals which each comprise 16-bits and compares the absolute values via comparator 46 to determine the larger one. The larger signal is selected and output by multiplexer 44 as a 16-bit result signal R_{BB}. The selection logic 48 checks for the first '1' bit and generates the appropriate selection control signal 58 which is applied to both I and Q multiplexers 50, 56, respectively. Both multiplexers have twelve 5-bit inputs comprising bits 15:11 through 4:0. The 5-bit output is passed through a limiter which functions to limit the values to ±15. Thus, a value of -16 is forced to -15. This is so that the absolute value function in the subsequent detector module does not generate +16 which would require 5-bits to represent, wherein the lookup table indexes are designed for 4-bits.

[0041]   The selection logic 48 will now be described in more detail. A pseudo code listing illustrating the selection logic portion of the baseband scaler in more detail is shown in Figure 3. Once the value R_{BB} (i.e. the larger of abs(I) and abs(Q) values) is determined, its position in the range of 1 to 2^{15} must be determined whereby the range is divided into slices of powers of 2, namely: 2^{15} to 2^{14}, 2^{14} to 2^{13}, 2^{13} to 2^{12}, ..., 2^5 to 2^4. The position of R_{BB} in a specific slice determines which bits of I and Q to route. For example, if R_{BB} belongs to the slice 2^{12} to 2^{11} 12, 11, 10, 9 and 8 of I and Q are to be routed. This ensures that the signal which is absolutely larger, will be in the range of 8 to 15 after scaling. Note that the logic selection is simplified since only the bits from MSB (not including the sign bit) to LSB in descending order need be examined. The pseudo code shown in Listing 1 (Figure 3) implements this scheme. Note that the scheme is scalable to any word length for I and Q of both input and output scaled values.

[0042]   The operation of the detector 26 (Figure 1) will now be described in more detail. A block diagram illustrating the arctan differential detector portion of the GFSK receiver in more detail is shown in Figure 4. The arctan differential detector, generally referenced 26, comprises I and Q absolute value blocks 60, 62, arctan lookup table 64, phase extractor 68, symbol delay 70, summer 72 and 'clicks' filter 74.

[0043]   The arctan differential detector is operative to extract the instantaneous phase using the scaled I and Q signals I_{SBB} and Q_{SBB}, respectively. The I and Q signals can be expressed as shown in Equation 1. The argument of both cosine and sine functions, denoted $\phi(t)$ is equivalent to the $\arctan\left(\dfrac{Q}{I}\right)$ as expressed below.

$$\phi(t) = \varphi(t) + \Delta\omega_{IF}t + \theta_n = \arctan\left(\frac{Q}{I}\right) \tag{5}$$

[0044] Assuming phase noise does not change much during a symbol time we can consider a constant phase noise θ_n, and the phase difference between two consecutive symbols can be expressed as

$$\phi(t) - \phi(t - T_S) = \Delta\varphi + \Delta\omega_{IF}T_S \qquad (6)$$

[0045] wherein T_S is the symbol time, $\Delta\varphi$ represents the differential phase and $\Delta\omega_{IF}T_S$ represents the frequency offset which is output as a DC offset level which can be compensated relatively easily using well known DC offset suppression techniques. The differential phase $\Delta\varphi$ is input to a 'clicks' filter which removes the discontinuities that occur around $\varphi = 2\pi$ radians.

[0046]   The main functional components of the arctan detector module are described below. The arctan lookup table (LUT) 64 is adapted to store 8-bit phase values φ for 0 to $\frac{\pi}{2}$ only (i.e. quadrant I > 0, Q > 0 only). The 2π phase extractor 68 functions to map the phase to the correct quadrant using the sign (i.e. the MSB) of the I and Q input scaled baseband signals, which the LUT does not use.

[0047]   A table illustrating the contents of the arctan LUT 64 is shown in Figure 5. The arctan lookup table receives as input the 4-bit magnitude of the scaled baseband I and Q signals. The abs() block 60 outputs the 4-bit magnitude of the scaled I baseband signal I_{SBB} while the abs() block 62 outputs the 4-bit magnitude of the scaled Q baseband signal Q_{SBB}, both of which are represented in two's complement form. Considering the lookup table as a matrix, then Q_{SBB} comprises the row index while I_{SBB} comprises the column index. For each (row, column) pair the lookup table is adapted to output an 8-bit representation for the value of $\arctan\left(\dfrac{Q_{SBB}}{I_{SBB}}\right)$. In general, the output size is preferably chosen such that a specific performance degradation criteria be met. In the example provided herein, the 8-bit representation was chosen to meet a performance degradation criteria of 0.2 dB loss in receiver sensitivity compared to an arbitrarily high number of bits per LUT word. It should be noted that the choice of a particular size could change once a receiver of such structure is to be used in a different application where the modulation scheme or performance requirements are different. Reducing the size permits reducing receiver size and cost but may compromise performance. Thus, there is an optimization procedure associated with the selection of the size at the time of design.

[0048]   Note that I_{SBB} and Q_{SBB} each comprise 5-bits and are limited in the baseband scaler to values of ±15 wherein -16 is not permitted. The abs() blocks output their magnitudes which function as the indices to the lookup table. The output of the lookup table is a two's complement 8-bit wide signal. Since each index can comprise one of 16 values (i.e. 0 to 15), it would appear that a matrix of $16 \times 16 = 256$ values is needed. Since the cases of row_index=0 and column_index=0 each yield a

constant value, however, then only $15 \times 15 = 225$ values are required in the matrix illustrated in Figure 5.

[0049]   The outputs resulting from the special cases of row_index=0 and/or column_index=0 are provided by pseudo code Listing 2 illustrated in Figure 6. This pseudo code listing handles the cases where the arctan argument is either zero or infinity (i.e. 90°). It is appreciated that one skilled in the art may generate an arctan LUT other than that shown herein in accordance with the desired index width. The 15 x 15 table illustrated herein fits within a 256 x 8 memory (only 225 bytes required, however). Depending on the width of each phase value and the width of the indices, a memory larger or smaller that that shown herein will be required.

[0050]   A graph of the I/Q plane illustrating the range covered by the arctan LUT is shown in Figure 7. The two crossing diagonal lines represent phase shifts in the modulated signal which result from the frequency deviations representing the modulating data. In the Bluetooth example provided herein, the nominal peak frequency deviations experienced for sufficiently long sequences of "0" or "1", are ±160 kHz, which over a single symbol duration of 1 μsec may create phase shifts of $\pm 2 \cdot \pi \cdot 160k \cdot 1 \mu sec = \pm 57.6°$. The received signal, however, may have frequency offsets as much as ±180 kHz, which could result in greater phase shifts over a symbol period. The hatched area in the first quadrant represents the range of phase values covered by the arctan LUT. The four points on the unit circle all represent the same phase output from the arctan LUT. The correct phase can only be determined by examining the signs of both the scaled I and Q baseband signals.

[0051]   A pseudo code listing illustrating the operation of the phase extractor portion of the arctan differential detector is shown in Figure 8. The pseudo code Listing 3 describes the logic implemented by the phase extractor module. Note that round(π*128) = 402, phi_base(k) is the value obtained from the arctan lookup table at indices $[abs(Q_{SBB}), abs(I_{SBB})]$ and phi(k) is the phase value output by the phase extractor.

[0052]   A differential phase value is then generated from the output of the phase extractor. The output of a one symbol delay 70 is subtracted from the current phase output to generate a differential phase value. This differential phase is then input to the clicks filter 74.

[0053]   A pseudo code listing illustrating the operation of the clicks filter portion of the arctan differential detector is shown in Figure 9. As described previously, discontinuities in the phase occur in the output of the phase extractor due to the wrapping of the phase around the -π to +π range. The discontinuity when moving from -π to +π or back generates much higher phase differences between symbols that cross this point (i.e. cause the phase to wrap around the -π to +π range) than expected by either the modulation or possible frequency offsets. The pseudo code Listing 4 in

Figure 9 functions to remove these 'clicks' or wrap arounds by checking for the conditions of delta_phi being greater than +π or less than -π. Note that the value of delta_phi cannot be much greater than $\Delta\varphi=\pm\pi\cdot h$, where h is the nominal modulation index (h = 0.32 according to the Bluetooth specification). This was shown above to be $\Delta\varphi_{max}=\pm57.6°$.

[0054]   The differential phase $\Delta\varphi$ output of the detector is input to the AFC module 28 (Figure 1). The function of the AFC block is to compensate for the influence of frequency deviations of the input spectrum from its intended center (i.e. the IF frequency) on the output data. It is noted that in the example implementation presented herein, the range of frequency offsets that must be handled is 125 kHz as implied by the Bluetooth specification (maximum of ±75 kHz of frequency error in the transmitter, and typically a ±20 ppm reference clock used for the 2.4 GHz local oscillator in the receiver, which can cause up to about ±50 kHz of additional frequency offset), plus ±40 kHz of drift allowed during long packet reception, plus ±15 kHz caused by inaccuracies in the A/D clock (for a specific implementation), for a total of ±180 kHz of possible frequency offset.

[0055]   Frequency offsets on the modulated signal are translated to DC offsets and added to the phase difference output of the differential detector. Thus, the role of the AFC is to estimate and compensate for the DC offset of the differential detector output. One possible scheme to estimate the DC offset is based on tracking the upper and lower peaks of the signal and calculating an average therefrom. The average is then subtracted from the signal to compensate for the offsets.

[0056]   The output of the AFC is input to the Adaptive Hard Decision Logic (AHDL)/Filter which is operative to make hard decisions based on the phase difference between two symbols. The AHDL can be implemented using well known slicing techniques or any other scheme that is able to recover the original data.

[0057]   It is noted that, in general, the number of words W_n in the LUT needed for a receiver based on the present invention could be $W_n=(N-1)^2$ if implemented as a ROM/RAM block, where N is the number of bits used to represent the I_{SBB} and Q_{SBB} signals. The total memory size M in bits would be $M = W_n \times W_s$, where W_s represents the word size (i.e. 8 in the example given herein). It is noted, however, that for a combinatorial logic based LUT (i.e. ROM function only), further reduction is possible by making use of the relationship $Memory(x,y) = S - Memory(y,x)$, which is equivalent to the trigonometric identity

$$\arctan\left(\frac{y}{x}\right) = 90° - \arctan\left(\frac{x}{y}\right) \tag{7}$$

wherein S represents the value for $90°$ $\left(\dfrac{\pi}{2}\,\text{radians}\right)$, and equals 201 in the example given in Figure

5. The diagonal of the LUT, where $x=y$ (or $I_{SBB}=Q_{SBB}$), corresponding to $\phi=45°$, is $Memory(x,x)=$ $round(S/2)$, which equals 101 in the example.

[0058]   The redundancy in the expression $Memory(x,y) = S - Memory(y,x)$, may be exploited by preceding the LUT with a function that would determine whether $I_{SBB}>Q_{SBB}$ and accordingly assigning either $x= I_{SBB}$ and $y=Q_{SBB}$ or $y= I_{SBB}$ and $x=Q_{SBB}$. If the LUT outputs the arctan(y/x), then for the latter a correction of the LUT output of $\phi = S - LUTout$ must be made.

[0059]   The LUT may be reduced further by replacing the diagonal with a single value that would be produced whenever the inputs x and y (scaled values for I and Q) are equal. The circuitry required to implement this reduction in LUT size would only be worthwhile in terms of gate count reduction above a certain word size N.

[0060]   It is intended that the appended claims cover all such features and advantages of the invention that fall within the spirit and scope of the present invention. As numerous modifications and changes will readily occur to those skilled in the art, it is intended that the invention not be limited to the limited number of embodiments described herein. Accordingly, it will be appreciated that all suitable variations, modifications and equivalents may be resorted to, falling within the spirit and scope of the present invention.